Amendments to the Specification:

Please replace the Title with the following replacement Title:

--METHOD FOR INTERLEAVING A PROGRAM OVER A PLURALITY OF CELLS--.

Please replace the abstract of the disclosure with the following amended abstract:

--For programming ~~Programming~~ of modules which can be reprogrammed during operation and for partitioning ~~is described. Partitioning~~ of code sequences, a control and/or data flow graph may be extracted from a program and separated into a plurality of subgraphs, which may be distributed among the modules ~~is also described~~. The separation of the flow graph may be such that connections between different ones of the subgraphs are minimized. During execution of the program, after a first module completes execution of a first part of one of the subgraphs, the first module may be reconfigured for execution of a first part of a second subgraph, while a second module executes a second part of the first subgraph.--.

Please replace the heading immediately preceding the first paragraph on page 1 with the following replacement heading:

--**Field of the Invention**--.

Please replace the heading immediately preceding the sixth paragraph on page 7 with the following replacement heading:

--**Detailed Description of the Invention**--.

Please replace the first paragraph on page 1 with the following replacement paragraph:

--The present invention may be applied to programmable arithmetic and/or logic hardware modules (Virtual Processing Units - VPUs) which can be reprogrammed during operation. For example, the present invention may be applied to VPUS having a plurality of arithmetic and/or logic units whose interconnection can also be programmed and reprogrammed during operation. Such logical hardware modules are available from several manufacturers under the generic name of FPGA (Field-Programmable Gate Arrays). Furthermore, several patents have been published, which describe special arithmetic

hardware modules having automatic data synchronization and improved arithmetic data processing.--.

Please replace the third paragraph on page 1 with the following replacement paragraph:

--The above described hardware modules may either have the units listed below or these units may be programmed or added (including externally):

1. at least one configuration unit (CT) for loading configuration data;
2. PAEs;
3. at least one interface unit ~~(IOAG)~~ for one or more memory(ies) and/or peripheral device(s).--.

Please replace the fifth paragraph on page 5 with the following replacement paragraph:

--Figure 18 illustrates an example complex machine in which the PAE array controls a load/store unit with a downstream Random Access Memory (RAM), according to an example embodiment of the present invention.--

Please replace the seventh paragraph on page 5 with the following replacement paragraph:

--Figure 20 illustrates the use of a memory in the First-In-First-Out (FIFO) mode, according to an example embodiment of the present invention.--.

Please replace the first complete paragraph on page 14 with the following replacement paragraph:

--The network of the status signals (0802) may represent a freely and specifically distributed status register of a single conventional processor (or of multiple processors of [[an]] a Symmetric Multiprocessing (SMP) computer). The status of each individual Arithmetic Logic Unit (ALU) (e.g., each individual processor) and, in particular, each individual piece of status information may be available to the ALU or ALUs (processors) that need the information. There is no additional program runtime or communication runtime (except for the signal runtimes) for exchange of information between the ALUs (processors).--.

Please replace the third paragraph on page 17 with the following replacement paragraph:

--The concept of VPU architecture may be extended. The virtual machine model may be used as a basis. The processing array of PAEs (PA) may be considered as an arithmetic unit with a configurable architecture. The CT(s) may represent a load unit (LOAD-UNIT) for opcodes. The interface units ~~IOAG(s)~~ may take over the bus interface and/or the register set.--.

Please replace the paragraph spanning pages 17 and 18 with the following replacement paragraph:

--1. A group of one or more PAEs may be configured to execute a complex command or command sequence and then the data associated with this command (which may be a single data word) is processed. Then this group is reconfigured to process the next command. The size and arrangement of the group may change. According to partitioning technologies described previously, it is the compiler's responsibility to create optimum groups to the greatest possible extent. Groups are "loaded" as commands onto the module by the CT; therefore, the method is comparable to the known Very Long Instruction Word (VLIW), except that considerably more arithmetic units are managed AND the interconnection structure between the arithmetic units can also be covered by the instruction word (Ultra Large Instruction Word = "ULIW"). This allows a very high Instruction Level Parallelism (ILP) to be achieved. (See also Fig. 27.) One instruction word corresponds here to one software module. A plurality of software modules can be processed simultaneously, as long as the dependence of the data allows this and sufficient resources are available on the module. As in the case of VLIW commands, usually the next instruction word is immediately loaded after the instruction word has been executed. In order to optimize the procedure in terms of time, the next instruction word can be pre-loaded even during execution (see Fig. 10). In the event of a plurality of possible next instruction words, more than one can be pre-loaded and the correct instruction word is selected prior to execution, e.g., by a trigger signal. (See Fig. 4a B1/B2, Fig. 15 ID C/ID K, Fig. 36 A/B/C.)--.

Please replace the first complete paragraph on page 18 with the following replacement paragraph:

--2. A group of PAEs (which can also be one PAE) may be configured to execute a frequently used command sequence. The data, which can also in this case be a

single data word, is sent to the group as needed and received by the group. This group remains without being reconfigured for a one or more. This arrangement is comparable with a special arithmetic unit in a processor according to the related art (e.g., multimedia extension (MMX)), which is provided for special tasks and is only used as needed. With this method, special commands can be generated according to the Complex Instruction Set Computer (CISC) principle with the advantage that these commands can be configured to be application-specific (Ultra-CISC = UCISC).--.

Please replace the fifth paragraph on page 19 with the following replacement paragraph:

--A memory within a VPU with PAE-like bus functions may represent various memory modes:

1. Standard memory (random access)
2. Cache (as an extension of the standard memory)
3. Lookup table
4. FIFO
5. Last-In-First-Out (LIFO) (stack).--.

Please replace the first complete paragraph on page 22 with the following replacement paragraph:

--The IO unit may be configured according to the peripheral requirements, for example:

1. Synchronous Dynamic RAM (SDRAM) controller
2. Rambus Dynamic RAM (RDRAM) controller
3. Digital Signal Processor (DSP) bus controller
4. Peripheral Component Interconnect (PCI) controller
5. serial controller (e.g., Next-Generation-Input-Output (NGIO))
6. special purpose controller (Small Computer Systems Interface (SCSI), Ethernet, Universal Serial Bus (USB), etc.).--.

Please replace the third complete paragraph on page 25 with the following replacement paragraph:

[[An]] A Memory Management Unit (MMU) can be associated with the external memory interface. The MMU may perform two functions:

1. Recompute the internal addresses to external addresses in order to support modern operating systems;
2. Monitor accesses to the external addresses, e.g., generate an error signal as a trigger if the external stack overruns or underruns.